CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (Original) A programmable multi-gigabit transceiver comprises:

programmable physical media attachment (PMA) module operably coupled to convert transmit parallel data into transmit serial data in accordance with a programmed serialization setting and to convert receive serial data into receive parallel data in accordance with a programmed deserialization setting;

programmable physical coding sublayer (PCS) module operably coupled to convert transmit data words into the transmit parallel data in accordance with a transmit interface setting and to convert the receive parallel data into receive data words in accordance with a receive interface setting;

programmable interface operably to convey the receive data words from the programmable PCS module to a programmable logic fabric section and to convey the transmit data words from the programmable logic fabric section to the programmable PCS module in accordance with a programmed logic interface setting; and

control module operably coupled to generate the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting based on a desired mode of operation for the programmable multi-gigabit transceiver.

2. (Original) The programmable multi-gigabit transceiver of claim 1, wherein the programmable PMA further comprises:

a programmable PMA receiver module operably coupled to deserialize the receive serial data in accordance with the programmed deserialization setting to produce the receive parallel data; and

a programmable PMA transmitter module operably coupled to serialize the transmit parallel data in accordance with a programmed serialization setting to produce the transmit serial data.

3. (Original) The programmable multi-gigabit transceiver of claim 2, wherein the programmable PMA receiver module further comprises:

programmable analog front-end operably coupled to amplify and equalize the receive serial data to produce amplified and equalized receive serial data, wherein amplification and equalization performed by the programmable analog front-end are set in accordance with the programmed deserialization setting;

data and clock recovery module operably coupled to recover data and a clock from the amplified and equalized receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the programmed deserialization setting; and

serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the programmed deserialization setting.

4. (Original) The programmable multi-gigabit transceiver of claim 2, wherein the programmable PMA transmitter module further comprises:

phase locked loop operably coupled to produce timing signals in accordance with the programmed serialization setting;

parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the timing signals, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the programmed serialization setting; and

driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the programmed serialization setting.

5. (Original) The programmable multi-gigabit transceiver of claim 1, wherein the programmable PCS module further comprises:

a programmable PCS receive module operably coupled to convert the receive parallel data into receive data words in accordance with the receive interface setting; and

a programmable PCS transmit module operably coupled to convert the transmit data words into the transmit parallel data in accordance with the transmit interface setting.

6. (Original) The programmable multi-gigabit transceiver of claim 5, wherein the programmable PCS receive module further comprises:

programmable data alignment module operably coupled to align the receive parallel data in accordance with the receive interface setting to produce aligned data words, wherein size and rate of the aligned data words are set based on the receive interface setting;

programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive interface setting to produce processed aligned data words, wherein the receive interface setting indicates descrambling, decoding, or passing of

the aligned data words, wherein the receive interface setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words;

programmable storage module operably coupled to elastic store or pass the processed data words in accordance with the receive interface setting to produce stored data words; and

programmable decode and verify module operably coupled to decode, verify or pass the stored data words in accordance with the receive interface setting and the programmed logic interface setting to produce the receive data words, wherein the receive interface setting indicates the decoding, the verifying or the passing of the stored data words, indicates a second type of decoding when the programmable decode and verify module is decoding the stored data words and indicates a type of verifying when the programmable decode and verify module is verifying the stored data words and wherein the programmed logic interface setting indicates rate and size of the received data words.

7. (Original) The programmable multi-gigabit transceiver of claim 5, wherein the programmable PCS transmit module further comprises:

programmable verify module operably coupled to verify or pass the transmit data words in accordance with the transmit interface setting and the programmed logic interface setting to produce verified transmit data words and wherein the programmed logic interface setting indicates size and rate of the transmit data words;

programmable encoding module operably coupled to encode or pass the verified transmit data words in accordance with the transmit interface setting to produce encoded data words, wherein the transmit interface setting indicates a type of encoding when the programmable encoding module is encoding the verified transmit data words;

programmable storage module operably coupled to elastic store or pass the encoded data words in accordance with the transmit interface setting to produce stored encoded data words; and

programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit interface setting to produce the transmit parallel data, wherein the transmit interface setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words.

8. (Original) The programmable multi-gigabit transceiver of claim 1 further comprises:

a PMA memory mapped register operable to store element settings for elements of the PMA module as indicated by the programmed serialization setting and the programmed deserialization setting; and

PCS register operable to store element settings for elements of the PCS module as indicated by the transmit and receive interface settings and the programmed logic interface setting.

9. (Original) The programmable multi-gigabit transceiver of claim 8, wherein the control module further functions to:

receive a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver;

convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting;

provide the programmed serialization setting and the programmed deserialization setting to the PMA memory mapped register; and

provide the transmit and receive interface settings and the programmed logic interface setting to the PCS register.

10. (Original) The programmable multi-gigabit transceiver of claim 8, wherein the control module further functions to:

determine a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver based on auto-configuration information;

convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive interface setting, the transmit interface setting, and the logic interface setting;

provide the programmed serialization setting and the programmed deserialization setting to the PMA memory mapped register; and

provide the transmit and receive interface settings and the programmed logic interface setting to the PCS register.

11. (Original) The programmable multi-gigabit transceiver of claim 1, wherein the control module further functions to:

generate the programmed serialization setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the programmable PMA module;

generate the programmed deserialization setting to enable, logically disable, or physically disable at least one element of a programmable PMA transmit module of the programmable PMA module;

generate the transmit interface setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the programmable PCS module; and

generate the receive interface setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the programmable PCS module.

12. (Currently Amended) A programmable logic device comprises:

clock management module operably coupled to provide a reference clock from one of a plurality of clock sources;

transmit physical media attachment (PMA) module operably coupled to convert parallel transmit data into serial transmit data, wherein the transmit PMA module receives the parallel transmit data in accordance with a parallel transmit clock and transmits the serial transmit data in accordance with a serial transmit clock, wherein the transmit PMA module generates the parallel transmit clock, the serial transmit clock, and a transmit programmable logic clock based on the reference clock;

receive PMA module operably coupled to convert serial receive data into parallel receive data, wherein the receive PMA module receives the serial receive data in accordance with a serial receive clock and provides the parallel receive data in accordance with a parallel receive clock, wherein the receive PMA module generates the serial receive clock, the parallel receive clock, and a receive programmable logic clock based on the reference clock;

transmit physical coding sublayer (PCS) module operably coupled to convert transmit data words into the parallel transmit data in accordance with the parallel transmit clock;

receive PCS module operably coupled to convert the parallel receive data into receive data words in accordance with the parallel receive clock; [[and]]

programmable logic fabric operably coupled to produce the transmit data words in accordance with the transmit programmable logic clock and to process the received data words in accordance with the receive programmable logic clock; and

wherein the plurality of clock source further comprises a low jitter external clock source, a recovered clock, and internal clock of the programmable logic fabric.

13. (Cancelled)

14. (Original) The programmable logic device of claim 12, wherein the reference clock further comprises:

a transmit reference clock that is provided to the transmit PMA module, wherein the transmit PMA module generates the serial transmit clock and the parallel transmit clock based on the transmit reference clock; and

a receive reference clock that is provided to the receive PMA module, wherein the receive PMA module generates the serial receive clock and the parallel receive clock based on the receive reference clock.

15. (Original) The programmable logic device of claim 12, wherein the receive PMA module further comprises:

programmable analog front-end operably coupled to amplify and equalize the serial receive data to produce amplified and equalized serial receive data, wherein amplification and equalization performed by the programmable analog front-end are set in accordance with a programmed deserialization setting;

data and clock recovery module operably coupled to recover data and a clock from the amplified and equalized serial receive data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the programmed deserialization setting, wherein the phase locked loop generates the serial receive clock, parallel receive clock, and the receive programmable logic clock based on the recovered clock and the reference clock; and

serial-to-parallel module operably coupled to convert the recovered data into the parallel receive data, wherein rate of the parallel receive data and width of the parallel receive data are set in accordance with the programmed deserialization setting.

16. (Original) The programmable logic device of claim 12, wherein the transmit PMA module further comprises:

phase locked loop operably coupled to produce the serial transmit clock, the parallel transmit clock, and the transmit programmable logic clock based on the reference clock in accordance with a programmed serialization setting;

parallel-to-serial module operably coupled to convert the parallel transmit data into a serial data stream based on the serial transmit clock and the parallel transmit clock, wherein data width of the parallel transmit data and rate of the serial data stream are set in accordance with the programmed serialization setting; and

driver operably coupled to drive the serial data stream on to a transmission line as the serial transmit data, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the programmed serialization setting.

17. (Original) The programmable logic device of claim 12, wherein the receive PCS module further comprises:

programmable data alignment module operably coupled to align data words of the parallel receive data in accordance with a receive interface setting and the parallel transmit clock to produce aligned data words, wherein size and rate of the aligned data words are set based on the receive interface setting;

programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive interface setting to produce processed aligned data words, wherein the receive interface setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive interface setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words;

programmable storage module operably coupled to elastic store or pass the processed data words in accordance with the receive interface setting to produce stored data words; and

programmable decode and verify module operably coupled to decode, verify or pass the stored data words in accordance with the receive interface setting and a programmed logic interface setting to produce the receive data words, wherein the receive interface setting indicates the decoding, the verifying or the passing of the stored data words, indicates a second type of decoding when the programmable decode and verify module is decoding the stored data words and indicates a type of verifying when the programmable decode and verify module is verifying the stored data words and wherein the programmed logic interface setting indicates rate and size of the received data words.

18. (Original) The programmable logic device of claim 12, wherein the transmit PCS module further comprises:

programmable verify module operably coupled to verify or pass the transmit data words in accordance with a transmit interface setting and a programmed logic interface setting to produce verified transmit data words and wherein the programmed logic interface setting indicates size and rate of the transmit data words;

programmable encoding module operably coupled to encode or pass the verified transmit data words in accordance with the transmit interface setting to produce encoded data words, wherein the transmit interface setting indicates a type of encoding when the programmable encoding module is encoding the verified transmit data words;

programmable storage module operably coupled to elastic store or pass the encoded data words in accordance with the transmit interface setting to produce stored encoded data words; and

programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit interface

setting to produce the parallel transmit data, wherein the transmit interface setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words.

19. (Currently Amended) A programmable multi-gigabit transceiver comprises:

a transmit section operably coupled to convert transmit data words into transmit serial data in accordance with a transmit setting;

a receive section operably coupled to convert receive serial data stream into receive data words in accordance with a receive setting;

an interface to programmable logic section operably coupled to provide the transmit data words from the programmable logic section to the transmit section in accordance with the transmit setting and to receive the receive data words from the receive section in accordance with the receive setting; and

control module operably coupled to produce the transmit setting and the receive setting based on transceiver operational requirements; and

wherein the control module further functions to:

generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the receiver section;

generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PMA transmit module of the transmit section;

generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the transmit section; and

generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the receive section.

20. (Original) The programmable multi-gigabit transceiver of claim 19, wherein the transmit section further comprises:

a programmable physical coding sublayer (PCS) transmit module operably coupled to convert the transmit data words into transmit parallel data in accordance with the transmit setting; and

a programmable physical media attachment (PMA) transmit module operably coupled to serialize the transmit parallel data in accordance with the transmit setting to produce the transmit serial data.

21. (Original) The programmable multi-gigabit transceiver of claim 20, wherein the programmable PMA transmit module further comprises:

phase locked loop operably coupled to produce timing signals in accordance with the transmit setting;

parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the transmit setting, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the transmit setting; and

driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the transmit setting.

22. (Original) The programmable multi-gigabit transceiver of claim 20, wherein the programmable PCS transmit module further comprises:

programmable verify module operably coupled to verify or pass the transmit data words in accordance with the transmit setting to produce verified transmit data words and wherein the transmit setting indicates size and rate of the transmit data words;

programmable encoding module operably coupled to encode or pass the verified transmit data words in accordance with the transmit setting to produce encoded data words, wherein the transmit setting indicates a type of encoding

when the programmable encoding module is encoding the verified transmit data words;

programmable storage module operably coupled to elastic store or pass the encoded data words in accordance with the transmit setting to produce stored encoded data words; and

programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit setting to produce the transmit parallel data, wherein the transmit setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words.

23. (Original) The programmable multi-gigabit transceiver of claim 19, wherein the receive section further comprises:

a programmable physical media attachment (PMA) receive module operably coupled to convert the receive serial data into receive parallel data in accordance with the receive setting; and

a programmable physical coding sublayer (PCS) receive module operably coupled to convert the receive parallel data into the receive data words in accordance with the receive setting.

24. (Original) The programmable multi-gigabit transceiver of claim 23, wherein the programmable PMA receive module further comprises:

programmable analog front-end operably coupled to amplify and equalize the receive serial data to produce amplified and equalized receive serial data, wherein amplification and equalization performed by the programmable analog front-end are set in accordance with the receive setting;

data and clock recovery module operably coupled to recover data and a clock from the amplified and equalized receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the receive setting; and

serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the receive setting.

25. (Original) The programmable multi-gigabit transceiver of claim 23, wherein the programmable PCS receive module further comprises:

programmable data alignment module operably coupled to align the receive parallel data in accordance with the receive setting to produce aligned data words, wherein size and rate of the aligned data words are set based on the receive setting;

programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive setting to produce processed aligned data words, wherein the receive setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words;

programmable storage module operably coupled to elastic store or pass the processed data words in accordance with the receive setting to produce stored data words; and

programmable decode and verify module operably coupled to decode, verify or pass the stored data words in accordance with the receive setting and the programmed logic interface setting to produce the receive data words, wherein the receive setting indicates the decoding, the verifying or the passing of the stored data words, indicates a second type of decoding when the programmable decode and verify module is decoding the stored data words and indicates a type of verifying when the programmable decode and verify

module is verifying the stored data words and wherein the programmed logic interface setting indicates rate and size of the received data words.

26. (Original) The programmable multi-gigabit transceiver of claim 19, wherein the control module further functions to:

receive a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver; and

convert the programming setting into the receive setting and the transmit setting.

27. (Cancelled)

28. (Original) A programmable logic device comprises:

a plurality of programmable multi-gigabit transceivers, wherein each of the plurality of programmable multi-gigabit transceivers is individually programmed to a desired transceiving mode of operation in accordance with a plurality of transceiver settings to transceive data;

programmable logic fabric operably coupled to the plurality of programmable multi-gigabit transceivers, wherein the programmable logic fabric is configured to process at least a portion of the data; and

control module operably coupled to produce the plurality of transceiver settings based on a desired mode of operation of the programmable logic device.

29. (Original) The programmable logic device of claim 28, wherein each of the plurality of programmable multi-giga bit transceivers further comprises:

programmable physical media attachment (PMA) module operably coupled to transmit parallel data into transmit serial data in accordance with a programmed serialization setting of a corresponding one of the plurality of transceiver settings and to convert receive serial data into receive parallel data in accordance with a programmed deserialization setting of the corresponding one of the plurality of transceiver settings;

programmable physical coding sublayer (PCS) module operably coupled to convert transmit data words into the transmit parallel data in accordance with a transmit PMA_PCS interface setting of the corresponding one of the plurality of transceiver settings and to convert the receive parallel data into receive data words in accordance with a receive PMA_PCS interface setting of the corresponding one of the plurality of transceiver settings; and

programmable interface operably to convey the receive data words from the programmable PCS module to the programmable logic fabric section and the convey the transmit data words from the programmable logic fabric section to the programmable PCS module in accordance with a programmed logic interface setting, wherein the control module generates the programmed serialization setting, the programmed deserialization setting, the receive PMA_PCS interface setting, the transmit PMA_PCS interface setting, and the logic interface setting based on a desired mode of operation for the programmable multi-gigabit transceiver.

30. (Original) The programmable logic device of claim 29, wherein the programmable PMA further comprises:

a programmable PMA receiver module operably coupled to convert the receive serial data into the receive parallel data in accordance with the programmed deserialization setting; and

a programmable PMA transmitter module operably coupled to convert the transmit parallel data into the transmit serial data in accordance with a programmed serialization setting.

31. (Original) The programmable logic device of claim 30, wherein the programmable PMA receiver module further comprises:

programmable analog front-end operably coupled to amplify and equalize the receive serial data to produce amplified and equalized receive serial data, wherein amplification and equalization performed by the

programmable analog front-end are set in accordance with the programmed deserialization setting;

data and clock recovery module operably coupled to recover data and a clock from the amplified and equalized receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the programmed deserialization setting; and

serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the programmed deserialization setting.

32. (Original) The programmable logic device of claim 30, wherein the programmable PMA transmitter module further comprises:

phase locked loop operably coupled to produce timing signals in accordance with the programmed serialization setting;

parallel-to-serial module operably coupled to convert the transmit parallel data into the transmit serial data based on the timing signals, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the programmed serialization setting; and

driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the programmed serialization setting.

33. (Original) The programmable logic device of claim 29, wherein the programmable PCS module further comprises:

a programmable PCS receive module operably coupled to convert the receive parallel data into the receive data words in accordance with the receive PMA_PCS interface setting; and

a programmable PCS transmit module operably coupled to convert the transmit data words into the transmit parallel data in accordance with the transmit PMA_PCS interface setting.

34. (Original) The programmable logic device of claim 33, wherein the programmable PCS receive module further comprises:

programmable data alignment module operably coupled to align the receive parallel data in accordance with the receive PMA_PCS interface setting to produce aligned data words, wherein size and rate of the aligned data words are set based on the receive PMA_PCS interface setting;

programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive PMA_PCS interface setting to produce processed aligned data words, wherein the receive PMA_PCS interface setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive PMA_PCS interface setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words;

programmable storage module operably coupled to elastic store or pass the processed data words in accordance with the receive PMA_PCS interface setting to produce stored data words; and

programmable decode and verify module operably coupled to decode, verify or pass the stored data words in accordance with the receive PMA_PCS interface setting and the programmed logic interface setting to produce the receive data words, wherein the receive PMA_PCS interface setting indicates the decoding, the verifying or the passing of the stored data words, indicates a second type of decoding when the programmable decode and verify module is decoding the stored data words and indicates a type of verifying when the programmable decode and verify module is verifying the stored data words and wherein the programmed logic interface setting indicates rate and size of the received data words.

35. (Original) The programmable logic device of claim 33, wherein the programmable PCS transmit module further comprises:

programmable verify module operably coupled to verify or pass the transmit data words in accordance with the transmit PMA_PCS interface setting and the programmed logic interface setting to produce verified transmit data words and wherein the programmed logic interface setting indicates size and rate of the transmit data words;

programmable encoding module operably coupled to encode or pass the verified transmit data words in accordance with the transmit PMA_PCS interface setting to produce encoded data words, wherein the transmit PMA_PCS interface setting indicates a type of encoding when the programmable encoding module is encoding the verified transmit data words;

programmable storage module operably coupled to elastic store or pass the encoded data words in accordance with the transmit PMA_PCS interface setting to produce stored encoded data words; and

programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit PMA_PCS interface setting to produce the transmit parallel data, wherein the transmit PMA_PCS interface setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words.

36. (Original) The programmable logic device of claim 29, wherein each of the programmable multi-gigabit transceivers further comprises:

a PMA memory mapped register operable to store element settings for elements of the PMA module as indicated by the programmed serialization setting and the programmed deserialization setting; and

PCS register operable to store element settings for elements of the PCS module as indicated by the transmit and receive PMA_PCS interface settings and the programmed logic interface setting.

37. (Original) The programmable logic device of claim 36, wherein the control module further functions to:

receive a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver;

convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive PMA_PCS interface setting, the transmit PMA_PCS interface setting, and the logic interface setting;

provide the programmed serialization setting and the programmed deserialization setting to the PMA memory mapped register; and

provide the transmit and receive PMA_PCS interface settings and the programmed logic interface setting to the PCS register.

38. (Currently Amended) The programmable logic device of claim[[38]] 36, wherein the control module further functions to:

determine a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver based on auto-configuration information;

convert the programming setting into the programmed serialization setting, the programmed deserialization setting, the receive PMA_PCS interface setting, the transmit PMA_PCS interface setting, and the logic interface setting;

provide the programmed serialization setting and the programmed deserialization setting to the PMA memory mapped register; and

provide the transmit and receive PMA_PCS interface settings and the programmed logic interface setting to the PCS register.

39. (Original) The programmable logic device of claim 29, wherein the control module further functions to:

generate the programmed serialization setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the programmable PMA module;

generate the programmed deserialization setting to enable, logically disable, or physically disable at least one element of a programmable PMA transceiver module of the programmable PMA module;

generate the transmit PMA_PCS interface setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the programmable PCS module; and

generate the receive PMA_PCS interface setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the programmable PCS module.

40. (Original) The programmable logic device of claim 28, wherein each of the plurality of programmable multi-gigabit transceivers further comprises:

a transmit section operably coupled to convert transmit data words into an transmit serial data in accordance with a transmit setting;

a receive section operably coupled to convert receive serial data stream into receive data words in accordance with a receive setting;

an interface to programmable logic fabric operably coupled to provide the transmit data words from the programmable logic fabric to the transmit section in accordance with the transmit setting and to provide the receive data words from the receive section to the programmable logic fabric in accordance with the receive setting; and

control module operably coupled to produce the transmit setting and the receive setting based on transceiver operational requirements.

41. (Original) The programmable logic device of claim 40, wherein the transmit section further comprises:

a programmable physical coding sublayer (PCS) transmit module operably coupled to convert the transmit data words into transmit parallel data in accordance with the transmit setting; and

a programmable physical media attachment (PMA) transmit module operably coupled to serialize the transmit parallel data in accordance with the transmit setting to produce the transmit serial data.

42. (Original) The programmable logic device of claim 41, wherein the programmable PMA transmit module further comprises:

phase locked loop operably coupled to produce timing signals in accordance with the transmit setting;

parallel-to-serial module operably coupled to convert the transmit parallel data into the receive serial data based on the transmit setting, wherein data width of the transmit parallel data and rate of the transmit serial data are set in accordance with the transmit setting; and

driver operably coupled to drive the transmit serial data on to a transmission line, wherein drive level of the driver and pre-emphasis settings of the driver is set in accordance with the transmit setting.

43. (Original) The programmable logic device of claim 41, wherein the programmable PCS transmit module further comprises:

programmable verify module operably coupled to verify or pass the transmit data words in accordance with the transmit setting to produce verified transmit data words and wherein the transmit setting indicates size and rate of the transmit data words;

programmable encoding module operably coupled to encode or pass the verified transmit data words in accordance with the transmit setting to produce encoded data words, wherein the transmit setting indicates a type of encoding when the programmable encoding module is encoding the verified transmit data words;

programmable storage module operably coupled to elastic store or pass the encoded data words in accordance with the transmit setting to produce stored encoded data words; and

programmable scrambling module operably coupled to scramble or pass the stored encoded data words in accordance with the transmit setting to produce the transmit parallel data, wherein the transmit setting indicates a type of scrambling when the programmable scrambling module is scrambling the stored encoded data words.

44. (Original) The programmable logic device of claim 40, wherein the receive section further comprises:

a programmable physical media attachment (PMA) receive module operably coupled to convert the receive serial data into receive parallel data in accordance with the receive setting; and

a programmable physical coding sublayer (PCS) receive module operably coupled to convert the receive parallel data into the receive data words in accordance with the receive setting.

45. (Original) The programmable logic device of claim 44, wherein the programmable PMA receive module further comprises:

programmable analog front-end operably coupled to amplify and equalize the receive serial data to produce amplified and equalized receive serial data, wherein amplification and equalization performed by the programmable analog front-end are set in accordance with the receive setting;

data and clock recovery module operably coupled to recover data and a clock from the amplified and equalized high-speed receive serial data to produce recovered data and a recovered clock, respectively, wherein the data and clock recovery module includes a programmable phase locked loop that is programmed in accordance with the receive setting; and

serial-to-parallel module operably coupled to convert the recovered data into the receive parallel data, wherein rate of the receive parallel data and width of the receive parallel data are set in accordance with the receive setting.

46. (Original) The programmable logic device of claim 44, wherein the programmable PCS receive module further comprises:

programmable data alignment module operably coupled to align the receive parallel data in accordance with the receive setting to produce aligned data words, wherein size and rate of the aligned data words are set based on the receive setting;

programmable descramble and decode module operably coupled to descramble, decode, or pass the aligned data words in accordance with the receive setting to produce processed aligned data words, wherein the receive setting indicates descrambling, decoding, or passing of the aligned data words, wherein the receive setting further indicates a type of descrambling when the programmable descramble and decode module is descrambling the aligned data words and further indicates a type of decoding when the programmable descramble and decode module is decoding the aligned data words;

programmable storage module operably coupled to elastic store or pass the processed data words in accordance with the receive setting to produce stored data words; and

programmable decode and verify module operably coupled to decode, verify or pass the stored data words in accordance with the receive setting and the programmed logic interface setting to produce the receive data words, wherein the receive setting indicates the decoding, the verifying or the passing of the stored data words, indicates a second type of decoding when the programmable decode and verify module is decoding the stored data words and indicates a type of verifying when the programmable decode and verify module is verifying the stored data words and wherein the programmed logic interface setting indicates rate and size of the received data words.

47. (Original) The programmable logic device of claim 40, wherein the control module further functions to:

receive a programming setting that indicates the desired mode of operation for the programmable multi-gigabit transceiver; and

convert the programming setting into the receive setting and the transmit setting.

48. (Original) The programmable logic device of claim 40, wherein the control module further functions to:

generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PMA receiver module of the receiver section;

generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PMA transceiver module of the transmit section;

generate the transmit setting to enable, logically disable, or physically disable at least one element of a programmable PCS transmit module of the transmit section; and

generate the receive setting to enable, logically disable, or physically disable at least one element of a programmable PCS receive module of the receive section.